IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Toshiharu Furukawa et al.	Confirmation No.:	6082
Art Unit:	2818		
Serial No.:	10/814,482		
Examiner:	David J. Goodwin		
Filed:	March 31, 2004		
Atty. Docket No.:	ROC9200300399US1		
For:	METHOD FOR FABRICATING STRAINED SILICON-ON-INSULATOR STRUCTURES AND STRAINED SILICON-ON-INSULATOR STRUCTURES FORMED THEREBY		

Cincinnati, Ohio 45202 Date: November 14, 2006

DECLARATION UNDER RULE 131

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We, Toshiharu Furukawa, Charles William Koburger, III, and James Albert Slinkman (the inventors), being duly cautioned and sworn, submit this Declaration in response to the Office Action dated October 18, 2006, and state:

That we are the inventors of the invention entitled "METHOD FOR FABRICATING STRAINED SILICON-ON-INSULATOR STRUCTURES AND STRAINED SILICON-ON-INSULATOR STRUCTURES FORMED THEREBY" described and claimed in the application for Letters Patent of the United States, Serial No. 10/814,482, filed March 31, 2004 (the '482 application);

That this is a Declaration under the provisions of Rule 131 and the rules of practice for the United States Patent Office in support of the '482 application;

That the invention described and claimed in the '482 application was conceived prior to April 29, 2003, the filing date of U.S. Patent Application Publication No. 2004/0217391 in the name of Forbes;

That, as evidence of the conception of the invention described and claimed in the '482 application, attached and incorporated into this Declaration as an Exhibit is a copy of a written invention disclosure, which bears dates (now masked), created by one or all of the undersigned inventors in the United States before April 29, 2003 and bearing a date before April 29, 2003 (but with said date now masked);

That the attached Exhibit includes a detailed description of a semiconductor structure, which clearly demonstrates that such semiconductor structure embodies the elements claimed in at least pending independent claim 1 of the '482 application, and which was conceived before the April 29, 2003 filing date of Forbes;

That the conception of the invention claimed in at least pending independent claim 1 of the '482 application is fully supported by the attached Exhibit, and that all drawings and text included in the Exhibit having been created in the United States by one or all of the undersigned inventors before the April 29, 2003 filing date of Forbes;

That the Exhibit demonstrates as follows:

That a semiconductor structure was conceived before April 29, 2003;

That the semiconductor structure comprised an island of a semiconductor material, said island including a plurality of sidewalls and a strained region; a handle wafer; and an insulating layer disposed between said island and said handle wafer, said insulating layer containing a thickened region underlying said strained region, said insulating layer electrically isolating said island of said semiconductor material from said handle wafer, and said thickened region transferring tensile stress to said strained region, as called for in the pending independent claim 1 in the '482 application;

That the undersigned inventors were diligent from before April 29, 2003, which represents the filing date of U.S. Patent Application Publication No. 2004/0217391, to March 31, 2004, which represents the filing date of the '482 application. Specifically, the undersigned inventors can account for the entire period during which reasonable diligence is required with affirmative acts within the United States and acceptable excuses. During this period, the attorneys acted within the United States with reasonable diligence on the application. Specifically, in-house counsel for the Assignee was reasonably diligent in considering the attached Exhibit prepared by the inventors and subsequently forwarding the attached Exhibit to outside counsel for the Assignee on November 13, 2003 with instructions to prepare a patent application on the subject matter of the Exhibit. Subsequently, outside counsel for the Assignee was reasonably diligent in preparing a working draft of specification the '482 application and forwarding the working draft of the specification to the inventors for their review on March 1, 2004. In particular, outside counsel for the Assignee had a reasonable backlog of unrelated cases taken up in chronological order and carried out expeditiously. The inventors were reasonably diligent in reviewing and approving the working draft of the specification between March 1, 2004 and March 16, 2004. Outside counsel for the Assignee was reasonably diligent in finalizing the specification of the '482 application, after receiving comments from the inventors' review, and forwarding the finalized specification to in-house counsel for the Assignee on March 16, 2004. In-house counsel for the Assignee was reasonably diligent in forwarding the specification for the '482 application and a Declaration/Power of Attorney to the inventors, who executed the Declaration/Power of Attorney on March 22, 2005 and March 25, 2005. In-house counsel for the Assignee was reasonably diligent in filing the '482 application and the executed Declaration/Power of Attorney at the U.S. Patent and Trademark Office on March 31, 2004;

Therefore, in summary, the Declaration and attached Exhibit constitute a showing of facts, in character and weight, that establish conception of the invention prior to the filing date of U.S. Patent Application Publication No. 2004/0217391 for a semiconductor structure that is the

subject of and is claimed in Application Serial No. 10/814,482, all the acts of which occurred in the United States BEFORE April 29, 2003, and thus precede the filing date of U.S. Patent Application Publication No. 2004/0217391, and that the inventors and counsel for the inventors exhibited diligence from prior to the filing date of April 29, 2003 of U.S. Patent Application Publication No. 2004/0217391 to the filing date of the '482 application.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Further declarants sayeth naught.

By _____
Toshiharu Furukawa

Date 11/14/2006

By _____
Charles William Koburger, III

Date November 14, 2006

By _____
James Albert Slinkman

Date _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Further declarants sayeth naught.

By_____
Toshiharu Furukawa

Date_____

By_____
Charles William Koburger, III

Date_____

By James Albert Slinkman
James Albert Slinkman

Date 11/16/2006

Disclosure ROC8-2003-0435

Prepared for and/or by an IBM Attorney -

Created By Charles Koburger III
Last Modified By Lisa Plank

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

***Title of disclosure (in English)**
Method for Fabricating Strained SOI Layers

Summary

Status		Submitted
Final Deadline		
Final Deadline Reason		
Original Location		BUR
*Processing Location		Rochester
*Functional Area	select	(1F) 1F - ETS - Engineering & Technology Services (Non-Rochester Inventors)
Attorney/Patent Professional		James R Nock/Rochester/IBM
IDT Team	select	James R Nock/Rochester/IBM
Submitted Date		
*Owning Division	select	ETS
Incentive Program		
Lab		
*Technology Code		101Wa
PVT Score		

Inventors with a Blue Pages entry

Inventors: Charles Koburger III/Fishkill/IBM, Toshiharu Furukawa/Burlington/IBM, James Slinkman/Burlington/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Koburger III, Charles W.	718628	21/JMJA		Hakey, Mark C.
Furukawa, Toshiharu	219417	29/BIXA		Sekiguchi, Akihisa (Aki)
Slinkman, James A.	061104	29/B5TV		Jaffe, Mark

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection

Attorney/Patent Professional	James R Nock/Rochester/IBM
IDT Team	James R Nock/Rochester/IBM
Response Due to IP&L	

*Main Idea

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

Stress in semiconductor substrate influences device characteristics. Tensile stress in the direction of current flow is known to increase performance of nFETs; copressive stress accomplishes the opposite.

	Ids delta Tensile stress parallel to Ids	Ids delta Tensile stress perpedicular to Ids	Ids delta Compressive stress parallel to Ids	Ids delta Compressive stress perpedicular to Ids
NFET	+	+	-	-
PFET	-	+	+	-

By controlling this stress one can improve technology performance.

Control of stress can be accomplished using Si-Ge alloys, by depositing insulating films with tailored stress, and by careful attention to thermal budgets and implant and salicidation conditions.

Adding additional methods for controlling stress will add options to the list of known available techniques. In many cases, other constraints on film properties make altering film deposition to tailor stress impossible.

Other references could include:

1) "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress," Greorgy Scott et al, 1999 IEDM Proceedings , pp 827-830.
(Comment: NMOS degraded by up to 13% by compressive stress in direction of current flow (perpendicular to PC).

2) "A New Aspect of Mechanical Stress Effects in Scaled MOS Devices,"
Akemi Hamada et al., IEEE Transactions on Electron Devices Vo;. 38 ,No. 4., April 1991, pp 895-900.
(Comment: Extraction of mobility behavior with externally applied stress.)

3) "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transisitor Design,"
Shinya Ito et al., 2000 IEDM Proceedings, pp. 247-250.
(Comment: NMOS degrades 8%, PMOS enhanced 7% by compressive stress (perpendicular to P).)

4) "A Highly Dense, High-Performance 130nm node CMOS Technology for Large-Scale System-on-a-Chip Applications," F. Ootsuka et al., 2000 IEDM Proceedings, pp. 575-578.
(Comment: Tensile stress of the contact Etch stop increases NFET IDsat by reducing STress due to bounding isolation.)

5) "Local Mechanical-Stress Control (LMC): A new Technique for CMOS-Performance Enhancement,"
A. Shimizu et. al., 2001 IEDM Proceedings. (ITIRC Search.) pp. ??
(Comment: Use of a SIN layer over silicide to modulate underlying RX stress. Stress can be tuned via variation of Ge II dose into the SiN layer.)

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.

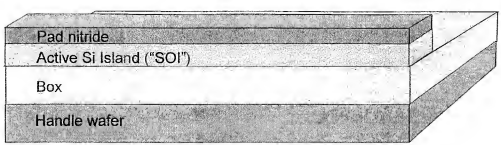
If active SOI islands are "stretched" by "pinning their ends" and "corrugating" the surface on which they lie, then they will be subject to increased tensile stress. We propose to accomplish this stretching by growing stripes of oxide in the BOX layer under the active silicon layer. When the ends of the islands cannot move (inward) to relax the strain, then tensile stress results.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

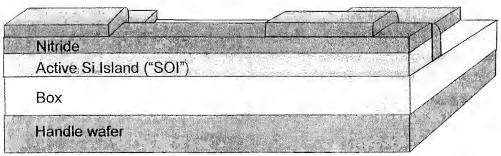
DrStrainLove.ppt

*Patent Value Tool

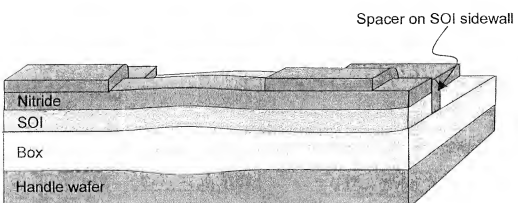
Proposal: Add tensile stress to a silicon line by pinning the ends and increasing the length of the path over which the line must lie by (basically) growing oxide on the silicon under the SOI "epi" layer. Think of a rubber band with ends held a fixed distance apart; push up in the middle. If you can't push up enough in one place, "corrugate" it with a series of bumps....



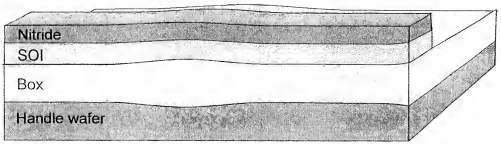
1. Start with usual SOI substrate after RX etch. Pad nitride remains in place. (View is cutaway of front.)



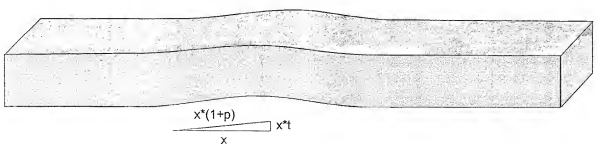
2. Deposit nitride. Mask to open windows through which oxidation in box to occur. Etch nitride using directional etch so spacers remain on sidewalls of "SOI" regions (to protect them from oxidation).



3. Oxidize to bulge SOI "upward" to stretch it.
If window width is 0.2 μm, then very rough estimate says that must grow approximately 4.5 nm of oxide to get 0.1% strain in silicon (see last page).



4. Strip thinner nitride.
   If doing STI, should pick nitride thicknesses so removal of window material will not erode pad significantly (or put thin oxide on top of pad to protect it from (thin) nitride removal).



Fit triangle to hump: $(1+p)^2=1+2p+p^2=1^2+t^2$.
If $p=10^{-3}$, then: $1+.002+.000001 = 1+t^2$. t=.045. So if x=100 nm, $x*t$=**4.5 nm**.
If stress/strain relaxes laterally, then will need to grow more.